REMARKS/ARGUMENTS

In view of the following remarks, Applicant respectfully requests reconsideration and allowance of the subject application. The actions taken herein place the Application in condition for allowance and Applicant respectfully requests that they be entered. No claims are amended. No claims are cancelled. New claims 24-25 are added. This amendment is believed to be fully responsive to all issues raised in the 10/19/04 Final Office Action.

CLAIM REJECTIONS

§103

Claims 1-3, 9, 13-14, 17 and 20 stand rejected under §103 as being unpatentable over US Patent No. 6,606,683 to Mori (hereinafter "Mori") in view of US Patent No. 6,151,641 to Herbert (hereinafter, "Herbert").

Claim 4 stands rejected under §103 as being unpatentable over US Patent No. 6,606,683 to Mori (hereinafter "Mori") in view of US Patent No. 6,151,641 to Herbert (hereinafter, "Herbert") in view of US Patent No. 5,659,718 to Osman (hereinafter "Osman").

Claims 5-8 stand rejected under §103 as being unpatentable over US Patent No. 6,606,683 to Mori (hereinafter "Mori") in view of US Patent No. 6,151,641 to Herbert (hereinafter, "Herbert") in view of US Patent No. 5,659,718 to Osman (hereinafter "Osman") and further in view of US Patent No. 5,142,683 to Burkhardt (hereinafter "Burkhardt").

Claims 10-11 and 18-19 stand rejected under §103 as being unpatentable over US Patent No. 6,606,683 to Mori (hereinafter "Mori") in view of US Patent No. 6,151,641 to Herbert (hereinafter, "Herbert") in view of US Patent No. 5,142,683 to Burkhardt (hereinafter "Burkhardt").

Claim 12 stands rejected under §103 as being unpatentable over US Patent No. 6,606,683 to Mori (hereinafter "Mori") in view of US Patent No. 6,151,641 to Herbert (hereinafter, "Herbert") in view of US Patent No. 5,142,683 to Burkhardt (hereinafter "Burkhardt") and further in view of US Patent No. 5,659,718 to Osman (hereinafter "Osman").

Claims 21-23 stand rejected under §103 as being unpatentable over US Patent No. 6,606,683 to Mori (hereinafter "Mori") in view of US Patent No. 6,151,641 to Herbert (hereinafter, "Herbert") in view of US Patent No. 5,675,807 to Iswandhi (hereinafter "Iswandhi").

Claim 1 is directed to a data array system for providing a host computer device having a host bus redundant access to a data storage device and recites:

- an active controller linked to the host bus and the data storage device, the active controller including a messaging mechanism for transmitting the messages and data over the host bus; and
- a standby controller linked to the host bus and the data storage device, the standby controller including message and data

buffers for storing the messages and data, whereby the host bus functions as an inter-controller-link.

The Office acknowledges that Mori does not disclose "the active controller and standby controller linked to the host bus whereby the host bus functions as an inter-controller-link". The Office then looks to Herbert for this limitation. Specifically, in the Final Office Action, the Office states, "Herbert teaches redundant controllers that attach directly to the host system's main PCI bus". The Office cites Herbert, col. 4, lines 32-40 in support of their position. Applicant respectfully disagrees that Herbert teaches or even contemplates "redundant controllers that attach directly to the host system's main PCI bus". The cited text of col. 4, lines 32-40 recites:

- In particular, the present invention is applicable to RAID controllers that attach directly to the host system's main bus (e.g., a PCI bus). The DMA controller of the RAID controller therefore completely controls the sequence of transfers directly from the host system's main memory on the PCI bus to the RAID controller local memory. Specifically, the DMA controller of the present invention enables the RAID subsystem controller to read data from the host at the subsystem's direction.

Consistently, the specification, claims, and drawings all teach a single RAID controller coupled to the host bus. Herbert is totally silent as to a

system utilizing multiple RAID controllers at all, much the less multiple RAID controllers coupled to a host bus.

Beyond the single RAID controller, Herbert teaches a DMA controller and a disk drive interface controller which are coupled within the RAID controller via a RAID controller internal bus 51. The internal bus is interfaced to the host PCI bus via a PC via bus bridge. See col. 8 lines 6-13. As such the host bus is only directly coupled to a single controller. Herbert does not contemplate multiple RAID controllers, or for that matter, multiple controllers of any type directly coupled to the host bus. Further, it follows that since Herbert is silent as to multiple controllers directly coupled with a host bus it does not contemplate a host bus which functions as an inter-controller-link as recited in claim 1.

Assuming arguendo that the Office is relying on the first sentence of the cited text which states "the present invention is applicable to RAID controllers that attach directly to the host system's main bus (e.g., a PCI bus)" for supporting that Herbert teaches multiple raid controllers, Applicant respectfully asserts that the Office is misconstruing the sentence. This sentence merely summarizes how the invention of Herbert relates to raid controllers. Neither the directly subsequent sentence, as described above, nor the remainder of the specification, the claims, nor the drawings suggest using multiple raid controllers, or multiple controllers of any kind for that matter directly connected to the host bus.

Even assuming arguendo that the cited text does relate to multiple raid controllers within a single system as the office suggests, Herbert contains no teachings as to how a host bus functions as an inter-controller-link as recited in claim 1.

Applicant respectfully disagrees with the Office's interpretation of Herbert; however, even accepting arguendo the Office's interpretation of Herbert, at least for the above reasons, the art of record still does not recite the limitations of claim 1. Applicant respectfully requests the §103 rejection of claim 1 be withdrawn.

Claims 2-8 depend from claim 1 and as such contain limitations not taught or suggested by the art of record. Therefore, Applicant respectfully requests the §103 rejection of claims 2-8 be withdrawn.

Claims 9-13 contain similar features to those of claim 1 which are not shown or suggested by the art of record. Applicant respectfully requests that the associated §103 rejection be withdrawn.

Claim 14 is directed to a data storage system with redundant data storage and recites:

- a host processor;
- an active controller controlling access by the host processor to data storage devices;
- a standby controller controlling access by the host processor to the data storage devices; and

- a host bus communicatively linking the host processor, the active controller, and the standby controller, wherein the active and standby controllers include redundancy messaging mechanisms configured to assert and sample signals on the host bus to provide inter-controller communications over the host bus.

The Office acknowledges that Mori does not disclose "a host bus communicatively linking the host processor, the active controller, and the standby controller, to assert and sample signals on the host bus to provide inter-controller communications over the host bus". The Office then looks to Herbert for this limitation and states that "Herbert teaches redundant controllers that attach directly to the host system's main PCI bus". Applicant respectfully disagrees with the Office's characterization of Herbert's teachings. Herbert teaches a system which utilizes a single RAID controller. The single RAID controller includes a DMA controller 71 and a disk drive interface controller 90. The DMA controller and the disk drive interface controller have distinct functionalities. Herbert does not characterize these controllers as active and standby. In this regard Herbert is non-analogous art with Mori. Even hypothesizing arguendo that the Office's characterization of Herbert is correct, the Office still has not provided any suggestion or motivation from the references as to why one of skill in the art would have been motivated to combine their teachings. At least for these reasons claim 14 is allowable over the art of record.

Neither Mori nor Herbert nor a combination thereof teach or describe "a host bus communicatively linking the host processor, the active controller, and the standby controller, wherein the active and standby controllers include redundancy messaging mechanisms configured to assert and sample signals on the host bus to provide inter-controller communications over the host bus" as recited in claim 14. At least for this additional reason Applicant respectfully requests that the §103 rejection of claim 14 be withdrawn.

Claims 15-20 depend from claim 14 and as such contain limitations not taught or suggested by the art of record. Therefore, Applicant respectfully requests the §103 rejection of claims 15-20 be withdrawn.

Claim 21 is directed to a method for providing inter-controller communications between an active controller and a standby controller configured for redundant communications between a host and a storage device and linked to a host bus, and recites:

- at the standby controller, specifying a range of memory in the standby controller as an interrupt range;
- with the active controller, writing data to the interrupt range of the standby controller; and
- at the standby controller, driving a local interrupt.

The Office admits that Mori and Herbert do not teach the limitations of claim 21 namely, "writing data to the interrupt range of the standby controller; and at the standby controller, driving a local interrupt". The Office then looks to Iswandhi for these limitations. The Office states that it would

have been obvious to combine these references. However, the Office does not provide any motivation or suggestion from the references for such a combination. Further, Iswandhi teaches directly away from the limitations of claim 21 in that it teaches a processing system composed of multiple sub-processing systems. Each sub-processing system has, as the main processing element, a central processing unit (CPU) that in turn comprises a pair of processors operating in lock-step, synchronized fashion to execute each instruction of an instruction stream at the same time. Col. 4 lines 44-50. In contrast, claim 21 is directed to an active controller and a standby controller performing distinct functions as evidenced from the limitations of claim 21, "at the standby controller, specifying a range of memory in the standby controller as an interrupt range", "with the active controller, writing data to the interrupt range of the standby controller", and "at the standby controller, driving a local interrupt".

The Office has failed to provide any motivation from the reference to combine the teachings of the art of record. Further, the art itself teaches away from such a combination. As such the Office has failed to establish a prima facia §103 rejection. Applicant respectfully requests that the §103 rejection of claim 23 be withdrawn.

Claims 22-23 depend from claim 21 and as such contain limitations not taught or suggested by the art of record. Therefore, Applicant respectfully requests the §103 rejection of claims 22-23 be withdrawn.

Applicant notes that the §103 rejections of the pending claims combine multiple references without sufficiently identifying the motivation to combine such references. Applicant specifically requests that the Office's support for such combinations be entered into the record to further prosecution of the present application.

NEW CLAIMS

New Claims 24-25 do not include new matter and are fully supported by the specification as originally filed.

Claim 24 is directed to a computing device and recites:

- a host central processing unit (CPU);
- a host bus communicatively coupled to the host CPU;
- at least one data storage device;
- an active controller linked to the host bus and the at least one data storage device, the active controller including a messaging mechanism for transmitting the messages and data over the host bus; and,
- a standby controller linked to the host bus and the at least one data storage device, the standby controller including message and data buffers for storing the messages and data, whereby the host bus functions as an inter-controller-link configured to transfer data and message information between the active and

standby controllers and wherein upon a failure of the active controller the inter-controller-link provides both data and message transfer within the computing device such that the host CPU can cause the standby controller to access data from the at least one data storage device.

The limitations of claim 24 are not taught or suggested by the art of record. Accordingly, Applicant respectfully requests that claim 24 be allowed.

Claim 24 is directed to a data array system for providing a host computer device having a host bus redundant access to a data storage device, and recites:

- an active controller sub-system linked directly to the host bus and the data storage device, the active controller sub-system including a messaging mechanism for transmitting messages and data over the host bus; and,
- a standby controller sub-system linked directly to the host bus and the data storage device, the standby controller sub-system including message and data buffers for storing the messages and data, whereby the host bus functions as a redundant inter-controller-link such that upon failure of either of the active controller subsystem and the standby controller sub-system the

host computing device maintains access to the data storage device.

The limitations of claim 25 are not taught or suggested by the art of record. Accordingly, Applicant respectfully requests that claim 25 be allowed.

Conclusion

Claims 1-25 are believed to be in condition for allowance. Applicant respectfully requests reconsideration and prompt issuance of the present application. Should any issue remain that prevents immediate issuance of the application, the Examiner is encouraged to contact the undersigned attorney to discuss the unresolved issue.

Respectfully Submitted,
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